

Electronics and PCB design

Reference for schematic capture, PCB layout, decoupling, power integrity, signal integrity, and the layer stack-up choices that determine yield and EMC outcome.

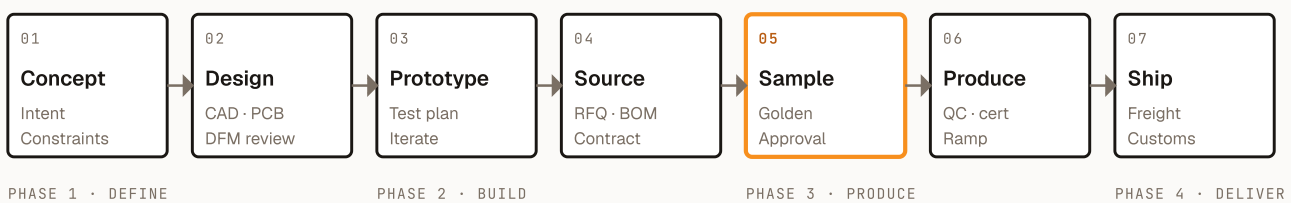
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ABSTRACT

PCB design is where electrical schematic intent becomes manufacturable geometry. Choices made at layout time — layer stack-up, decoupling strategy, ground topology, signal routing — determine whether the product passes EMC the first time, hits the yield target, and behaves consistently across the production batch.

Section 1 covers schematic best practices. Section 2 covers layer stack-up selection. Section 3 covers power and decoupling. Section 4 covers signal integrity and high-speed routing. Section 5 covers grounding and EMC layout. Section 6 covers design-for-manufacturing constraints and DRC rules.

HARDWARE PRODUCT DEVELOPMENT — 7-STAGE PIPELINE



PCB DESIGN SITS AT THE HEART OF PHASE 2 (BUILD). THE DECISIONS MADE HERE DETERMINE THE EMC, THERMAL, MANUFACTURING, AND FIELD-FAILURE PROFILE OF THE PRODUCT.

CONTENTS

- | | |
|-----------------------|----------------------------------|
| 1. Schematic capture | 4. Signal integrity + high-speed |
| 2. Layer stack-up | 5. Grounding + EMC layout |
| 3. Power + decoupling | 6. DFM + DRC |

1. Schematic capture

The schematic is the single source of truth for electrical intent. Layout follows; quality of layout depends entirely on quality of schematic.

1.1 Schematic hygiene

– Hierarchical structure

Group by function (power, MCU, sensors, comms, connectors). One sheet per functional block; 1–4 sheets typical for a 4-layer consumer board.

– Net naming conventions

Power nets in caps with voltage (`VDD_3V3` , `VBAT` , `GND`). Signal nets in mixed case (`SPI_CLK` , `I2C_SDA`). Differential pairs explicitly (`USB_DP` , `USB_DN`).

– Component reference designators

Sequential, mapped per IEEE Std 200 (R, C, L, U, Q, D, J, Y, etc.).

– Pin numbering on every component

Including non-obvious mechanical (J1.MH for mounting hole tied to GND).

– Net labels everywhere

No floating wires. Labels visible at every termination.

1.2 Documentation per page

– Title block

Project, board name, schematic revision, designer, date, sheet X of Y.

– Off-page connectors

Named labels for inter-sheet signals.

– Revision history

Per page, dated changes.

– Components grouped visually

Sensor block, power section, MCU peripherals.

1.3 Bill of materials (BoM) alignment

– Schematic generates the BoM via design tool (Altium, KiCad, Eagle, OrCAD).

– Every component has an MPN + manufacturer in its properties.

– Critical components flagged (single-source, long-lead, allocated risk).

– Cross-check BoM count with reference designator count; mismatches indicate floating or duplicate components.

1.4 Design rules to check at schematic completion

CHECK	METHOD
Power supply currents balance	Sum max load across rails
All bypass capacitors per datasheet	One per VCC pin, one per power-rail bank
Pull-up/pull-down resistors per protocol	I2C: 1k-10k; USB: per spec; reset: 10k
All MCU pins assigned (no floating)	Tie unused to GND or VDD
Test points on all power rails + critical signals	Min 1 per net, more for ICT coverage
ESD protection on accessible ports	TVS arrays on USB-C, audio jacks, exposed contacts
Reset signal robustness	Watchdog + voltage supervisor on power-up
Boot mode selection visible	Bootloader pins available for programming

SCHEMATIC REVIEW CHECKLIST (60-MIN WALKTHROUGH)

A schematic review with a second engineer 1–2 weeks before layout freeze catches 80 % of issues that would otherwise surface at first prototype: - Each power rail traced end-to-end - Each bypass cap matched to datasheet (value, package, position) - ESD protection on every accessible signal - Reset network behaves correctly at power-up - Test points available for all rails + critical signals - BoM hygiene: no DNI components without rationale; no obsolete MPNs

2. Layer stack-up

The stack-up determines impedance, thermal performance, EMC behaviour, and manufacturability cost. Pick before routing.

2.1 Standard stacks for consumer hardware

STACK	LAYERS	USE	COST RELATIVE
2-layer (1.6 mm FR-4)	TOP / BOT	Simple logic, prototype	1×
4-layer (1.6 mm FR-4)	TOP / GND / VCC / BOT	Most consumer electronics	2–3×
6-layer (1.6 mm FR-4)	TOP / GND / SIG / SIG / VCC / BOT	RF, high-speed digital	4–6×
8-layer+	Mix per design	Complex SoC, BGA	6–10×
4-layer impedance-controlled	per spec	USB, MIPI, Ethernet	3–5×
HDI (high-density interconnect)	Microvias + buried	Smartphone, smartwatch	8–15×

2.2 When to go to 4 layers

- Component density: >10 components per cm²
- High-speed signals: USB 2.0+, Ethernet, MIPI, DDR
- Multiple voltage rails (3+ supplies)
- BGA packages (any size)
- EMC sensitivity (radio, sensor inputs, audio)

2.3 Layer assignment for 4-layer board

“ TOP layer: Components + short signal routing GND layer: Solid ground plane (no splits) PWR layer: Power planes (can have multiple voltage zones) BOT layer: Routing + some components (BGA fanouts) ”

Common error: routing power on the GND layer. Don't do this — break the ground plane and lose return-path integrity.

2.4 Standard impedance reference

TRACE TYPE	WIDTH × SPACING × THICKNESS	IMPEDANCE
Single-ended 50 Ω (FR-4, 4-layer, 0.20 mm dielectric)	0.30 mm	50 Ω
Single-ended 50 Ω (FR-4, 4-layer, 0.10 mm dielectric)	0.18 mm	50 Ω
Differential 90 Ω (USB 2.0)	0.12 mm × 0.20 mm gap	90 Ω diff
Differential 100 Ω (Ethernet, LVDS)	0.13 mm × 0.18 mm gap	100 Ω diff
Coplanar waveguide (RF)	Width tuned per stack	50 Ω (Z ₀)

Verify with your supplier's impedance calculator (Polar SI9000, Saturn PCB, manufacturer-specific tool).

3. Power + decoupling

Power integrity decisions made at layout time are nearly impossible to fix in production. Get them right at the start.

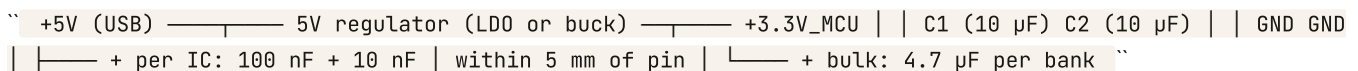
3.1 Decoupling capacitor selection

FREQUENCY RANGE	CAPACITOR TYPE	TYPICAL VALUE	PLACEMENT
<1 kHz (line ripple)	Electrolytic / tantalum	10–100 μ F	Near regulator output
1 kHz – 1 MHz (switching ripple)	Ceramic X7R	0.1–10 μ F	Per power-supply pin bank
1 MHz – 100 MHz (RF, fast switching)	Ceramic X5R / NPO	10 nF – 100 nF	Adjacent to IC power pins
100 MHz – 1 GHz (RF, decoupling)	Ceramic NPO	1 nF – 10 nF	Multiple per power pin
>1 GHz	High-Q resonators	10 pF – 100 pF	RF design specific

3.2 Bypass cap placement rules

- One ceramic 100 nF per VCC pin of every IC. Within 5 mm of the pin.
- One bulk cap (1–10 μ F) per power-rail bank (e.g., per side of an FPGA, per regulator).
- Multiple ceramics in parallel (10 nF + 100 nF + 1 μ F) at high-current IC pins (MCU, comms IC).
- Place caps on the bottom layer adjacent to the IC, with through-hole connection to power plane. Minimises return path length.

3.3 Power-rail decoupling diagram



3.4 Power supply considerations

- **LDO vs. buck regulator**
LDO if $V_{drop} < \sim 1$ V and current < 500 mA; buck for higher drop or current.
- **Quiescent current**
Critical for battery-powered designs. Look for < 10 μ A I_q in regulators.
- **Load step response**
Buck regulators have slower response; size output cap for transient.
- **Efficiency curve**
Look at efficiency vs. load. Often peaks at 50–70 % of rated.

3.5 Trace width for power

CURRENT	TRACE WIDTH (1 OZ CU, EXT)	TRACE WIDTH (2 OZ CU, EXT)
100 mA	0.30 mm	0.20 mm
500 mA	0.80 mm	0.50 mm
1 A	1.5 mm	0.8 mm
3 A	4.0 mm	2.5 mm
5 A	6.0 mm	4.0 mm

Internal layers carry ~50 % of external trace current at same width. Use IPC-2152 calculator for precise sizing.

POWER-RAIL AUDIT BEFORE LAYOUT FREEZE

Run this list 1 week before layout freeze: - Every IC's VCC pins have ceramic decoupling within 5 mm - Bulk capacitor per power-rail bank within 25 mm - Trace width supports max current (per IPC-2152) - Regulator output cap meets datasheet ESR requirement - High-current paths use multiple vias when going between layers - Return current path traced on the GND plane (no breaks)

4. Signal integrity + high-speed

High-speed signals (>100 MHz fundamental, or fast edge rates < 1 ns) need careful routing.

4.1 High-speed routing rules

- **Match trace lengths**

Within a differential pair: ± 0.1 mm. Within a parallel bus: ± 5 mm (DDR3) or per protocol.

- **Avoid stubs**

Stubs over $1/4$ wavelength of the signal frequency create reflections. Use vias for all branch connections.

- **Reference plane changes**

When transitioning between layers, place return-path vias adjacent to signal vias.

- **Avoid 90° bends**

Use 45° angles or curves. 90° creates impedance discontinuity.

- **Spacing between traces**

Coupling decreases as the cube of distance. 3W spacing reduces coupling by ~ 20 dB vs. 1W spacing.

4.2 Differential pair routing

- **Coupling**

Traces must be edge-coupled (close together) for full benefit of differential signaling.

- **Length matching**

Within a single pair: 0.1–0.5 mm typical, depending on data rate.

- **Skew matching**

Both traces should have the same number of vias, layer transitions, and bends.

- **Avoid asymmetric layouts**

One trace going around an obstacle while the other doesn't = skew.

4.3 Common high-speed signals

SIGNAL	FREQUENCY / DATA RATE	IMPEDANCE	LENGTH MATCH
USB 2.0	480 Mbps	90 Ω diff	± 0.15 mm
USB 3.0 / 3.1	5–10 Gbps	90 Ω diff	± 0.1 mm
Ethernet 100/1000	100/1000 Mbps	100 Ω diff	± 0.15 mm
MIPI CSI / DSI	Up to 6 Gbps	100 Ω diff	± 0.1 mm
DDR3 / DDR4	800–3200 Mbps	40–50 Ω SE	± 5 mm per byte lane
LVDS	Up to 1.5 Gbps	100 Ω diff	± 0.5 mm
HDMI	Up to 6 Gbps	100 Ω diff	± 0.1 mm

4.4 Crosstalk reduction

- **Spacing**

Maintain $3\times$ trace width (3W rule) between adjacent traces.

- **Routing layers**

Aggressors and victims on different layers when possible.

- **Guard traces**

Grounded traces between sensitive signals (rarely necessary in consumer designs).

- **Termination**

Series resistor (33–100 Ω) at the driver for fast logic outputs.

5. Grounding + EMC layout

Ground topology determines EMC performance and immunity. Most EMC failures trace back to ground design.

5.1 Ground strategies

- **Single ground plane**

Best for digital + low-frequency analog. Use solid copper pour on a dedicated layer.

- **Split ground**

Only when high-isolation needed (audio, sensitive analog). The split must be bridged at one point — typically near the ADC reference.

- **Star ground**

For mixed-signal designs. All grounds (analog, digital, chassis) connect at one point.

5.2 Common grounding mistakes

- **Splitting ground under high-speed traces**

Forces return current to take a long path; radiates strongly.

- **Cutting ground for thermal isolation**

Creates antenna-like structures.

- **No connection from chassis to PCB ground**

Static charge has no return path; ESD damage likely.

- **Multiple ground vias far apart**

Creates ground bounce. Add adjacent vias for low impedance.

5.3 EMC layout fundamentals

- **Minimise loop area**

Keep current loops small. Every signal trace has a return current; the loop area determines radiation.

- **Place sensitive circuits in low-noise zones**

Audio, ADC, antenna away from switching power supplies.

- **Shield switching power supplies**

Use a shielding can or keep the supply region tightly contained.

- **Ferrite beads on cables**

Add to USB, audio, and other cables to suppress conducted emissions.

- **Common-mode chokes on power inputs**

Reduces conducted emissions on power lines.

5.4 ESD protection

- **TVS diodes on every accessible signal**

USB-C, audio jack, switch inputs.

- **TVS placement**

At the connector, not at the IC. Clamps the surge before it propagates.

- **Bidirectional TVS**

For AC signals (audio).

- **ESD test rating**

IEC 61000-4-2: ±8 kV contact / ±15 kV air for level 4.

6. DFM + DRC

Manufacturing rules that prevent yield problems. Set these in the design tool.

6.1 Standard DRC rules

PARAMETER	STANDARD	PREMIUM
Trace / space	0.20 mm / 0.20 mm	0.125 mm / 0.125 mm
Annular ring (PTH)	0.20 mm	0.15 mm
Drill diameter (vias)	0.30 mm	0.20 mm (laser: 0.10 mm)
Aspect ratio	8:1	10:1
Soldermask dam	0.10 mm	0.075 mm
Silkscreen line width	0.15 mm	0.10 mm
Min text height	0.8 mm	0.6 mm
Edge-to-copper	0.20 mm	0.20 mm
Pad-to-pad	0.15 mm	0.10 mm

6.2 Component placement rules

- **Component-to-component spacing**
Minimum 0.5 mm SMD, 1 mm for hand-rework accessibility.
- **Orientation consistency**
Group similar components in same orientation to reduce machine-vision verification time and AOI false-positives.
- **Polarity markings**
Capacitors, diodes, ICs clearly marked on silkscreen.
- **Fiducial marks**
Three global fiducials (preferred) or two diagonal. Local fiducials for 0402 + finer or BGA.
- **Test points**
1.0 mm diameter pads, 2.54 mm spacing for ICT. At least one per net.
- **Keep-out zones**
1 mm around connectors, 2 mm around antennas, 3 mm around shielding cans.

6.3 Production-readiness checklist

- All Gerber files generated and verified in CAM viewer
- Drill file matches PCB design
- Pick-and-place file (X, Y, rotation per component)
- BoM in supplier's preferred format
- Assembly drawing with PCB dimensions + critical mechanical features
- Stencil file for SMT
- Test point report for ICT
- Panelization details (V-score lines, tabs, mouse-bites)
- Soldermask + silkscreen artwork verified

FINAL NOTE. PCB design is a discipline of trade-offs. Every routing decision affects EMC, thermals, yield, and cost. The best PCB designs start with a clear schematic, a deliberate stack-up choice, and a rigorous DRC. The worst PCBs are routed in a hurry; they reveal their problems in batches of failed lab tests and field returns six months later.